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Application Note
AN 21-002

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Gate Driver Basics

1. Introduction

This application note is intended to assist in the selection and implementation of an off-the-shelf driver core or plug-and-play gate driver. This application note replaces AN-7002, AN-7003, and AN-7004.

In power electronics systems, the term "gate driver" is generally used to describe the circuit connecting the low-voltage controller (containing software and system logic) to the high-voltage power modules (containing IGBTs, MOSFETs, etc.).

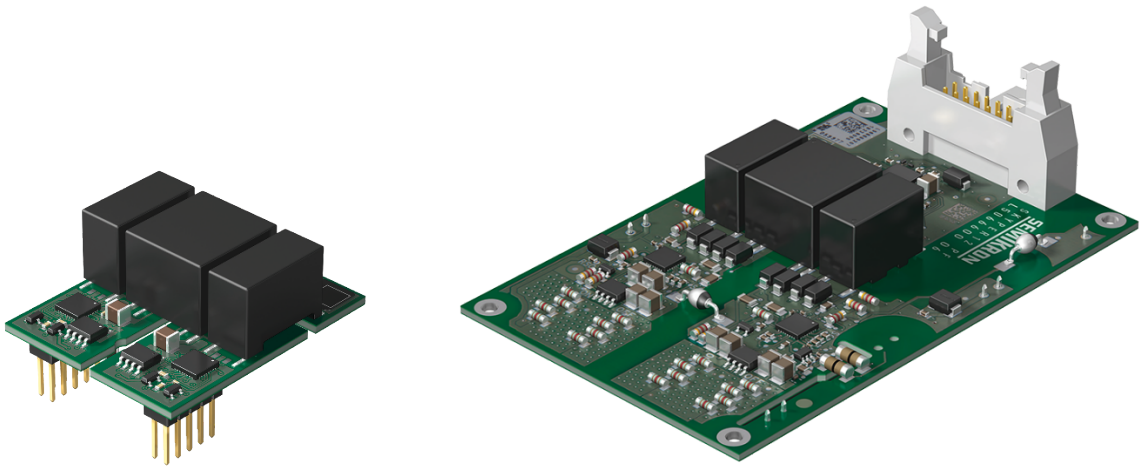
Commercial IGBT/MOSFET drivers are available in three basic classes:

- **Driver ICs:** This term covers the broad category of integrated circuits from basic level shifters (e.g. 3.3V logic input, high current bipolar output) to complete driver circuits integrating logic and isolation into one transfer-moulded package. In the former case, these components require the design of

additional isolation and/or power supply circuits to achieve full functionality. In the latter case, due to the physical constraints of the package, these devices are generally limited to lower power applications.

- **Driver cores:** For medium to high power applications, a driver core (Figure 1L) provides all of the functional blocks of a complete driver IC, but on a larger scale. Isolation is usually achieved with large optocouplers or pulse transformers that allow for higher operating voltages and greater creepage/clearance distances. The entire circuit is fabricated on a PCB that can be plugged/soldered into a larger PCB. This design allows flexibility to adjust gate resistance and trip levels for specific modules.
- **Plug-and-play:** For industry-standard modules (e.g. SEMITRANS10, SEMiX3p) complete driver boards (Figure 1R) containing all the features of a driver core plus the requisite gate resistors and configuration components for a specific module type are already installed. The PCBs are designed to directly press, solder, or plug into a certain module housing.

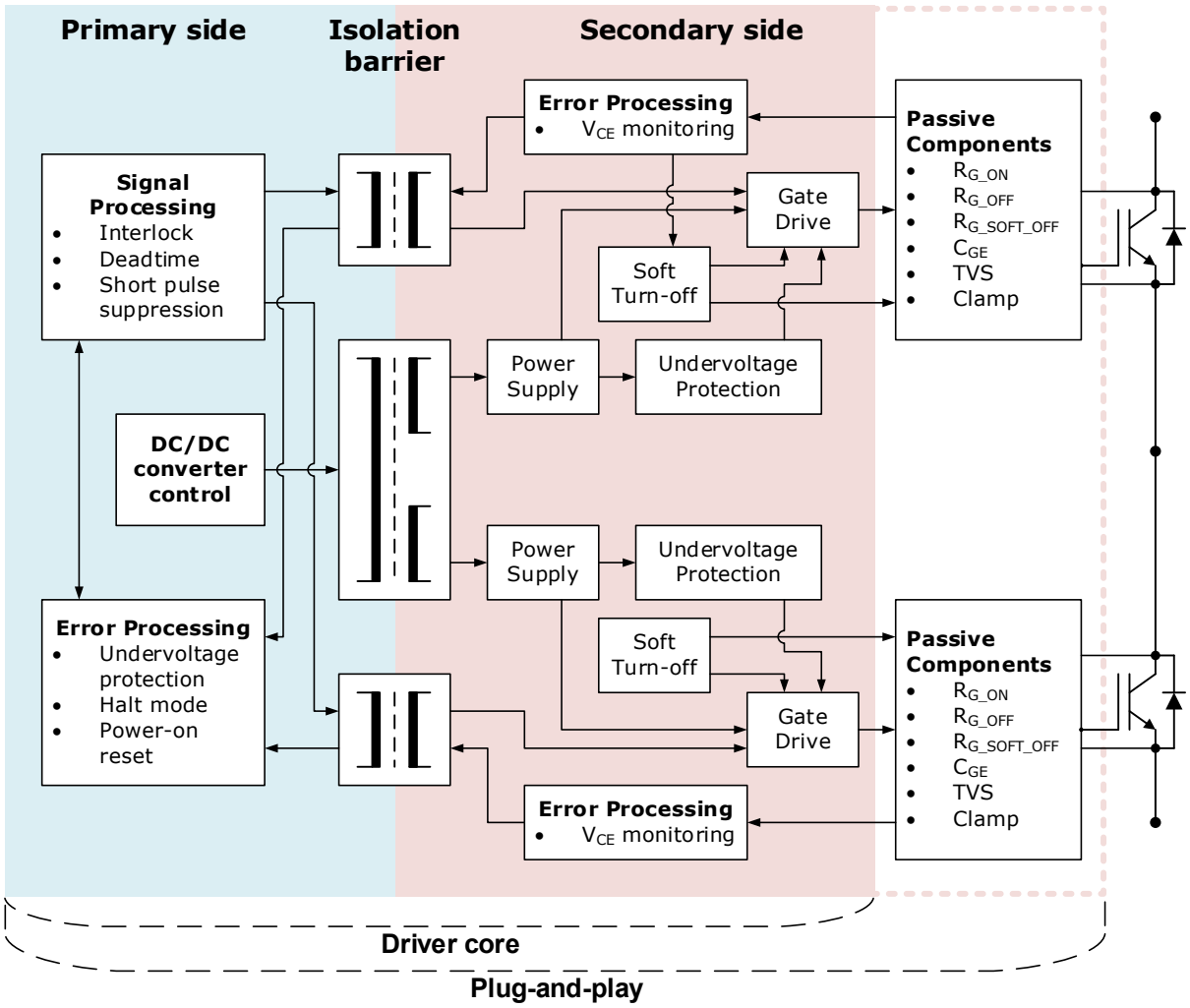
Figure 1: SKYPER 12 PV driver core (L) and SKYPER 12 press-fit plug-and-play driver for SEMiX3p module (R)



2. Topology

A modern two-channel driver circuit is generally constructed as in Figure 2 with the critical feature for safety being a clear delineation between primary (low voltage) and secondary (high voltage) sides. The controller is interfaced to the primary side, where logic (perhaps in the form of an ASIC) provides short pulse suppression, interlock and/or dead time, and generally conditions the gating signals so that they can be transmitted across an isolation barrier. Additionally, an isolated power supply is needed to provide the positive and negative voltage rails that are used to turn the power devices on and off. Secondary side components include this as well as fast-acting protection features (e.g. DSCP) that avoid the delay of sending an error and the ensuing turn-off signal across the isolation barrier.

Figure 2: SEMIKRON two-channel driver block diagram



2.1 Voltage rating

Most driver cores and plug-and-play drivers are categorized according to the maximum blocking voltage of the devices they are designed to drive (e.g. 1200V, 1700V). This rating, in turn, translates to the voltage used for type testing of the driver (V_{isol}) which is mainly determined by the isolation barrier between primary and secondary. Transformer-based isolation barriers, as used in most SEMIKRON driver products, are particularly robust in this regard with a typical isolation voltage rating of 4kVAC$_{rms}$. Relevant standards and methods for testing voltage isolation are given in [7].

3. Driver Output Capability

3.1 Drive voltage

While there are a variety of different techniques for turning a transistor gate on and off [2], by far the most common is the resistance-controlled voltage-source type. In this method, fixed turn-on and turn-off voltages are applied to the gate and the rate of rise of current is controlled with a resistor (Figure 3, Figure 4). Particularly for larger devices, separate turn-on and turn-off gate resistors are used and this will be assumed for most of the explanations given in this application note.

Figure 3: Turn-on of IGBT using a bipolar power supply for the gate driver

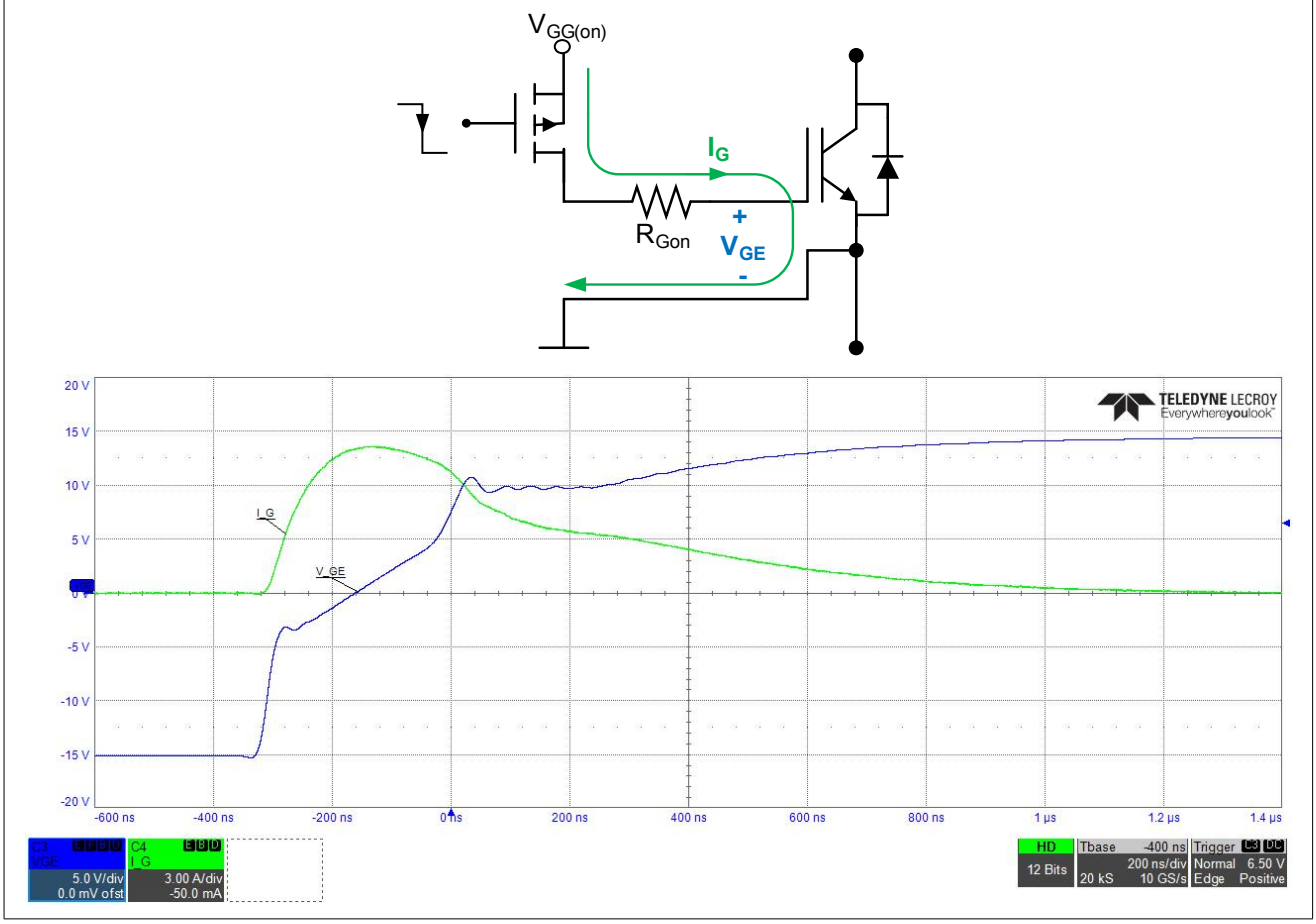
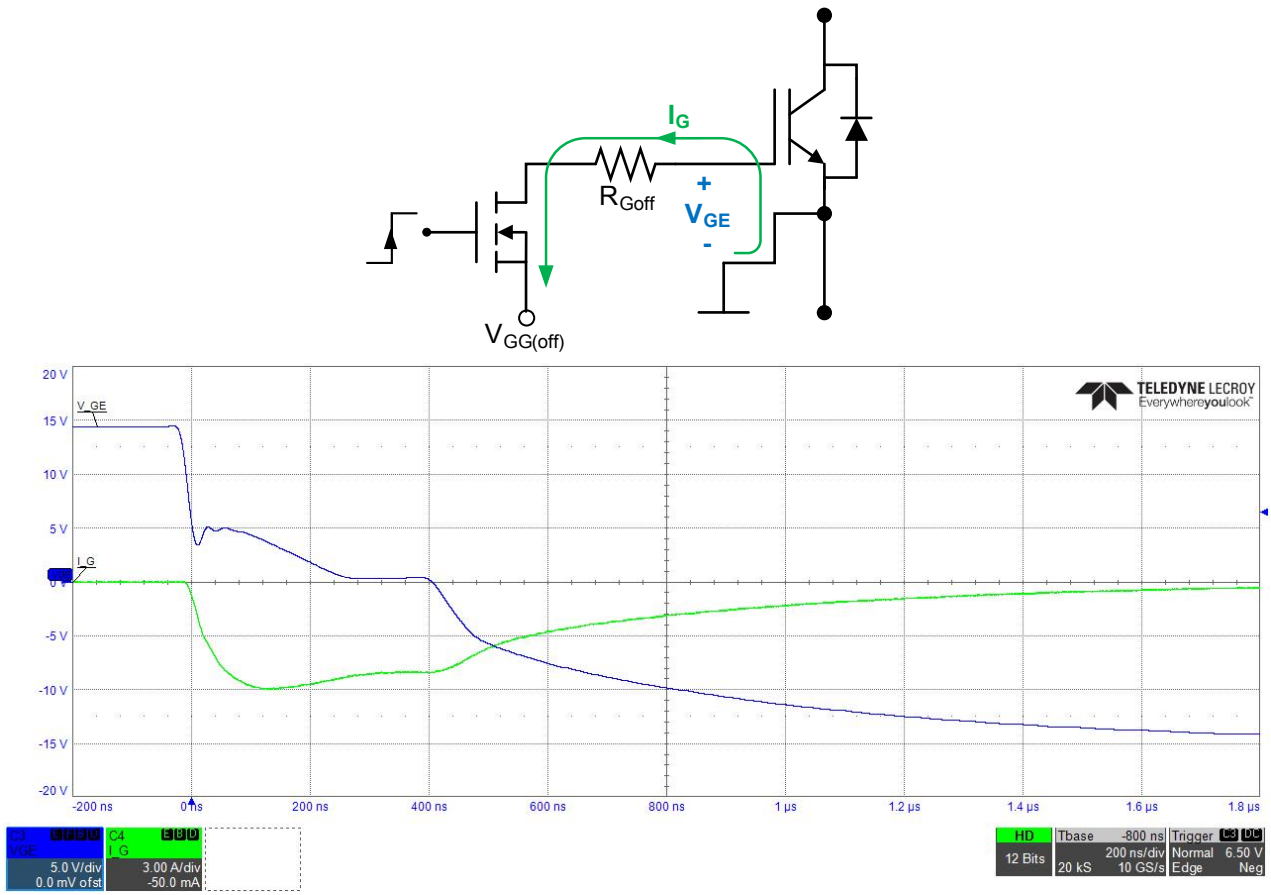


Figure 4: Turn-off of IGBT using a bipolar power supply for the gate driver



These turn-on and turn-off voltages are generally uniform for a given semiconductor technology and selected as a compromise between:

- Cost/complexity (bipolar vs. unipolar secondary-side voltage supplies)
- Switching speed
- Immunity to parasitic turn-on (see [3])
- Conduction losses (reducing $R_{DS(on)}$)
- Protecting the gate oxide (not exceeding V_{GES})

Silicon IGBTs are generally driven with a 15V turn-on voltage and a -5V…-15V turn-off voltage for larger (higher current) devices or 0V turn-off voltage for smaller (lower current devices). In the case of IGBT7 [6], it is possible to safely turn off even large devices using a 0V turn-off voltage due to the gate capacitance (i.e. C_{GE} is large relative to C_{GC}).

Silicon MOSFETs are generally driven with a 10V…15V turn-on voltage and a 0V turn-off voltage.

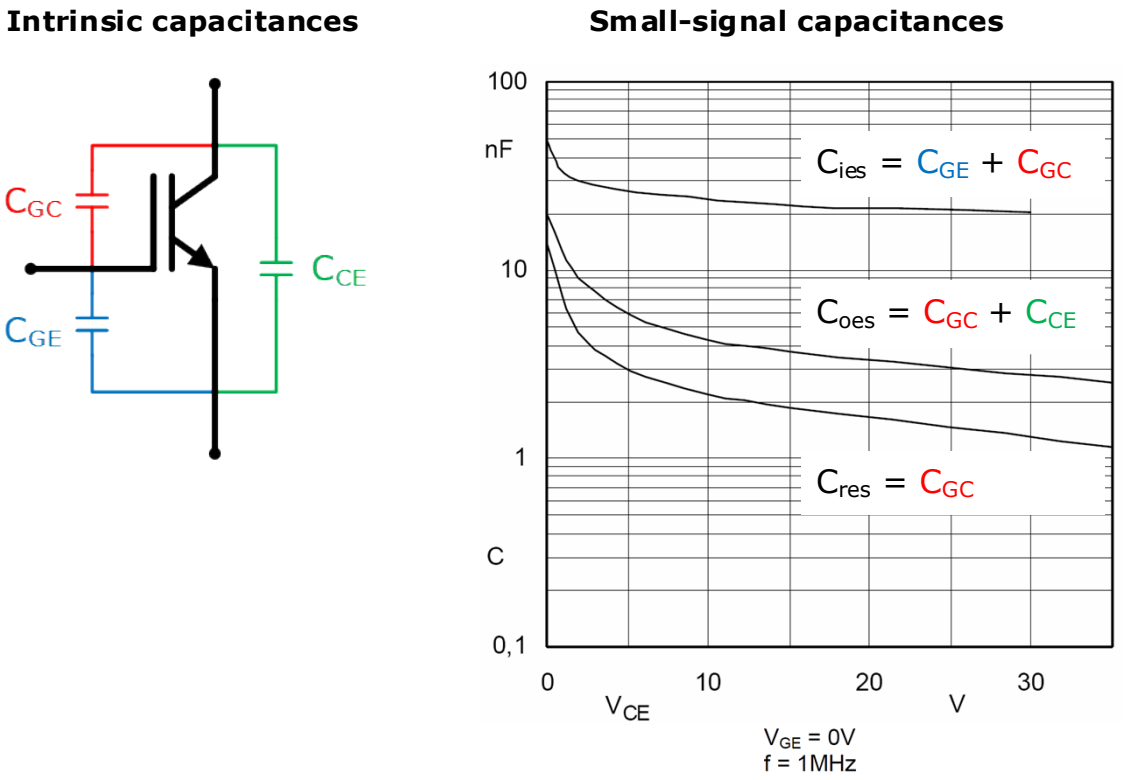
Silicon carbide MOSFETs are still evolving at the time of this writing but generally are driven with a high (15V…20V) turn-on voltage to reduce on-state losses. A slightly negative turn-off voltage (-3V…-5V) is recommended.

In most cases, these turn-on/turn-off voltages are fixed for off-the-shelf driver solutions so it is only necessary to be aware of the used voltages when looking at other datasheet values (e.g. Q_G).

3.2 Gate charge

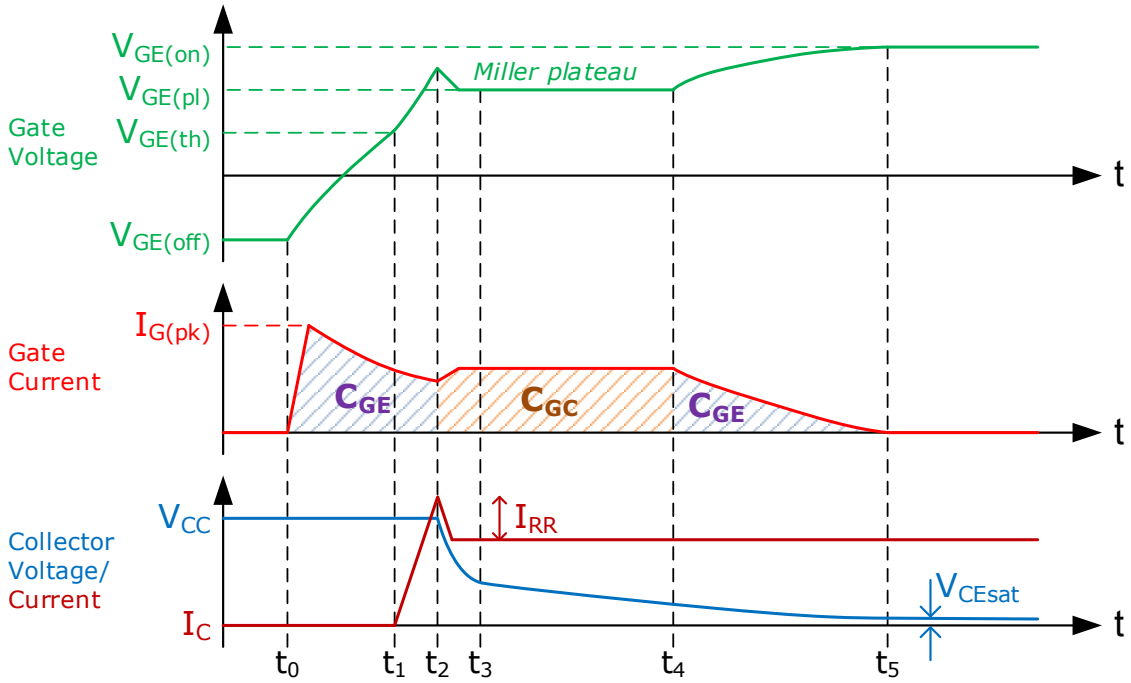
The fabrication of any insulated gate transistor (IGBT, MOSFET) yields three main intrinsic capacitances (C_{GE}, C_{CE}, C_{GC}). These capacitances can be combined to form general "small signal capacitances" (C_{ies}, C_{res}, C_{oes}) and vary with voltage applied across the transistor.

Figure 5: Intrinsic and small-signal capacitances



For gate driver sizing, the most important of these capacitances are C_{GE} ("gate capacitance") and C_{GC} ("Miller capacitance") as they most strongly determine the gate voltage and current characteristics. Figure 6 shows the idealized waveforms at the gate including which capacitances are being charged by the gate current.

Figure 6: Idealized gate turn-on waveforms



The main intervals of interest are (terms given for an IGBT):

t_0…t_1: The gate current I_G charges the input capacitance C_{GE} and the gate-emitter voltage V_{GE} rises to the threshold voltage $V_{GE(th)}$. Depending on the gate resistor, several amperes may be running in this state. As V_{GE} is still below $V_{GE(th)}$, no collector current flows during this period and V_{CE} remains at V_{CC}.

t_1…t_2: As soon as V_{GE} exceeds $V_{GE(th)}$, the main device turn-on process starts. I_C begins to increase but since the free-wheeling diode is still conducting current at the beginning of this interval (for most topologies), the collector-emitter voltage V_{CE} will not yet drop. The reverse recovery behaviour of the free-wheeling diode causes overshoot in the collector current (I_{RR}). While the device is in the active mode, the gate voltage is directly linked to the collector current so the overshoot is reflected in the gate waveforms.

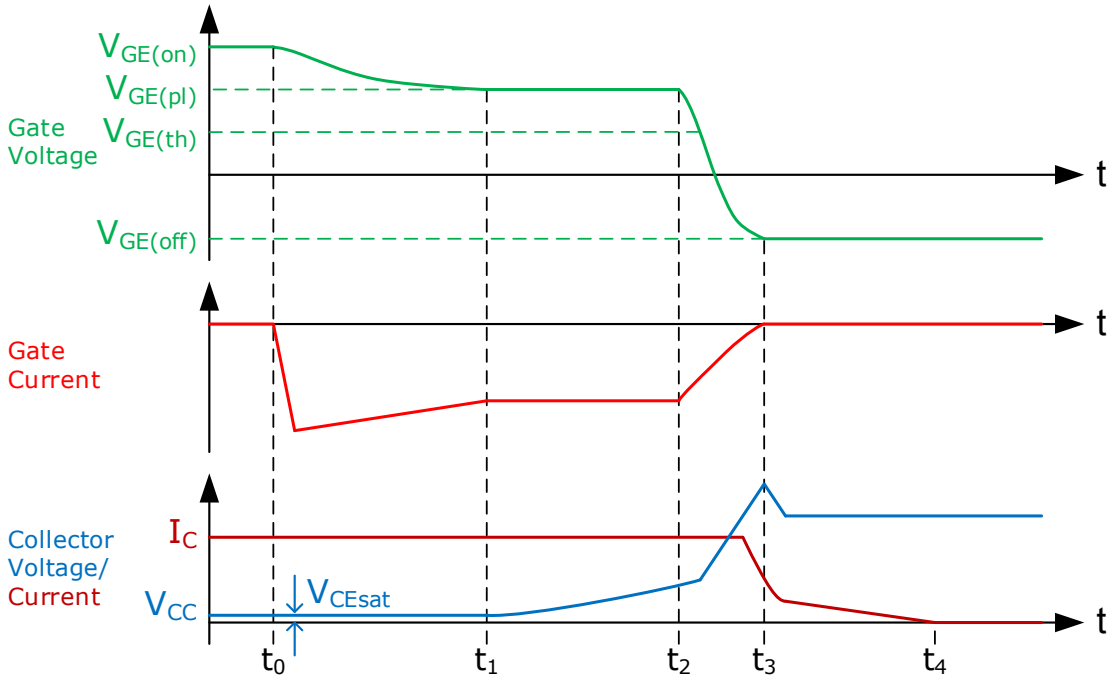
t_2…t_3: When the free-wheeling diode is finally off, V_{CE} starts to drop rapidly and dV_{CE}/dt is high. V_{GE} is held to $V_{GE(pl)}$ as C_{GC} charges, resulting in the characteristic "Miller plateau".

t_3…t_4: V_{CE} decreases at a slower rate (with increasing C_{GC} and constant gate current) towards the on-state value (V_{CEsat}) as C_{GC} continues to charge. V_{GE} remains at $V_{GE(pl)}$.

t_4…t_5: At the beginning of this interval, the device is fully turned-on. With C_{GC} finally charged, C_{GE} is now able to completely charge, resulting in V_{GE} reaching its steady state value, $V_{GE(on)}$. V_{CE} reaches the on-state value, V_{CEsat}.

Turn-off of the device gate involves discharging the capacitances in a very similar manner. Idealized turn-off waveforms (valid for the larger gate resistances typically used in applications) are given in Figure 7.

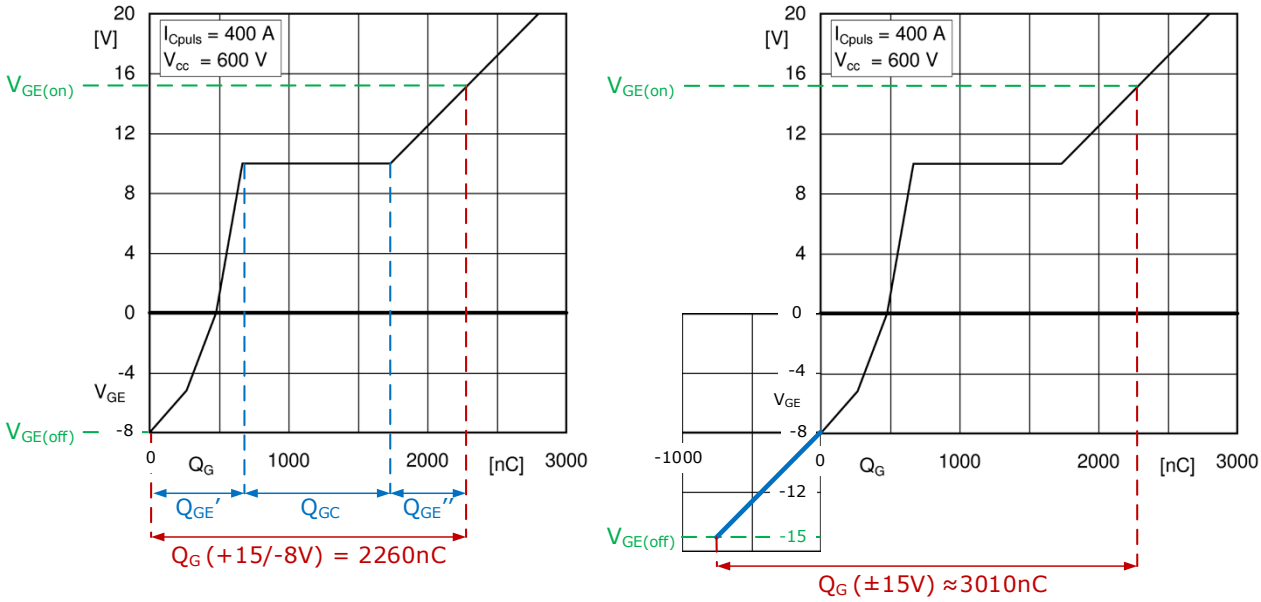
Figure 7: Idealized gate turn-off waveforms



While the capacitances described in Figure 5 influence the switching characteristics of the device, they are not used directly to size the driver. For that, the gate charge characteristic is used. This characteristic is given in the module datasheet in the form of a graph showing how the gate voltage changes with accumulated charge (Figure 8L). The effective gate charge is then measured from the turn-off voltage, $V_{GE(off)}$, to the turn-on voltage, $V_{GE(on)}$. As this voltage can vary between drivers, this should be checked before reading the effective gate charge, Q_G.

In some cases, the datasheet graph may not extend far enough to account for the implemented gate voltages. In this case, the gate charge characteristic should be extrapolated to determine the higher effective gate charge (Figure 8R).

Figure 8: Example gate charge characteristic from SKM400GB12E4 datasheet (L) and extrapolation method (R)



3.2.1 Q_{out} and additional boost capacitance

The gate driver must be able to source or sink the gate charge every switching event without a significant drop of the voltage at the secondary-side power supply (e.g. +15V, -8V). A drop in this voltage during switching can lead to increased switching losses. Because of this, gate driver datasheets give a value for maximum output charge per pulse, Q_{out}, which must be above the value of Q_G determined above. However, the datasheet Q_{out} is often given with the caveat that some additional boost capacitance must be added to the by the user. The method for calculating this capacitance is given in the respective Technical Explanations for the driver (e.g. SKYPER 42 LJ). Capacitors are placed on the secondary side in parallel with both the TOP (e.g. 15V) and BOT (e.g. -8V) connections and should be close to the driver power supply pins. It is strongly recommended that these be ceramic type and electrolytic or tantalum types are to be avoided. Additionally, drivers may require that the additional secondary-side capacitance be duplicated on the primary side as well.

3.3 Average gate current

With the gate charge for a given device determined, the required average current can be calculated as:

$$I_{G(avg)} = f_{sw} \cdot Q_G \qquad (1)$$

Where:

$I_{G(avg)}$: Required average gate current in Amperes
f_{sw}: IGBT/MOSFET switching frequency in Herz
Q_G: IGBT/MOSFET gate charge in Coulombs (for a given voltage change)

The driver datasheet gives the value $I_{out(avg)}$, the average output current capability per channel. Therefore, the calculated value $I_{G(avg)}$ must be smaller than $I_{out(avg)}$, which may be derated with temperature.

Similarly, the average output power required can be calculated by factoring in the total available gate voltage:

$$P_{G(avg)} = I_{G(avg)} \cdot \left(V_{GE(on)} - V_{GE(off)}\right) \qquad (2)$$

3.4 Peak gate current

The peak current that occurs in the gate circuit during every turn-on or turn-off event can be roughly calculated using the driving voltage and the total resistance in the gate circuit. In reality, the inductance in

the gate circuit further limits the current but since it may not be known during the initial design stages, the absolute worst-case peak current can be estimated as:

$$I_{G(pk)} = \frac{V_{GE(on)} - V_{GE(off)}}{R_G + R_E + R_{Gint}} \quad (3)$$

Where:

R_G: Externally applied turn-on (or turn-off) gate resistor
R_E: Externally applied emitter resistor, if present
R_{Gint}: Gate resistor internal to module

The driver datasheet gives the value $I_{out(peak)}$, the peak output current capability per channel. Therefore, the calculated value $I_{G(pk)}$ should be below $I_{out(peak)}$, though due to the worst-case nature of the calculated current (mentioned previously) this should only be considered for rough selection of the driver.

4. Gate Resistor

As explained above, on a basic level the gate resistor controls the charging and discharging of a (gate) capacitance. This, in turn, affects a number of critical parameters:

- Device switching time
- Switching losses
- Reverse bias safe operating area (RBSOA)
- Short-circuit safe operating area (SCSOA)
- Electromagnetic (high-frequency) emissions
- Rate of change of collector-emitter (drain-source) voltage, dv/dt
- Rate of change of collector (drain) current, di/dt
- Reverse recovery of free-wheeling diode

This behaviour can vary between technologies (IGBT/MOSFET "generations"), but in general an increased gate resistance will lead to slower switching speed and increased switching losses. Gate resistance selection is a trade-off between maximum allowed voltage slopes (dv/dt), EMI, and switching losses.

4.1 Minimum gate resistance

When an IGBT (MOSFET) module is qualified by a manufacturer, switching tests are performed to determine the turn-on and turn-off resistors that will minimize switching losses while also maintaining stable behaviour across the safe operating area for the device. This is done in a controlled environment with standardized equipment and a low-inductance DC-link structure. The resulting minimum recommended resistor values (and corresponding switching speeds and losses) are given in the "Characteristics" section of the device datasheet (Figure 9). While these values can be taken as a starting point, the optimal gate resistor for a given application can only be found through double-pulse testing [4].

Figure 9: Location of minimum turn-on and turn-off resistors in datasheet (SKM400GB12E4)

$t_{d(on)}$	V_{CC} = 600 V I_C = 400 A V_{GE} = ±15 V $R_{G\ on}$ = 1 Ω $R_{G\ off}$ = 1 Ω di/dt_{on} = 9700 A/µs di/dt_{off} = 4300 A/µs	T_j = 150 °C	242	ns
t_r		T_j = 150 °C	47	ns
E_{on}		T_j = 150 °C	33	mJ
$t_{d(off)}$		T_j = 150 °C	580	ns
t_f		T_j = 150 °C	101	ns
E_{off}		T_j = 150 °C	56	mJ

Maximum gate resistance is not defined, but cannot be so large as to keep the device from reaching saturation during each switching period (i.e. linear operation is prohibited).

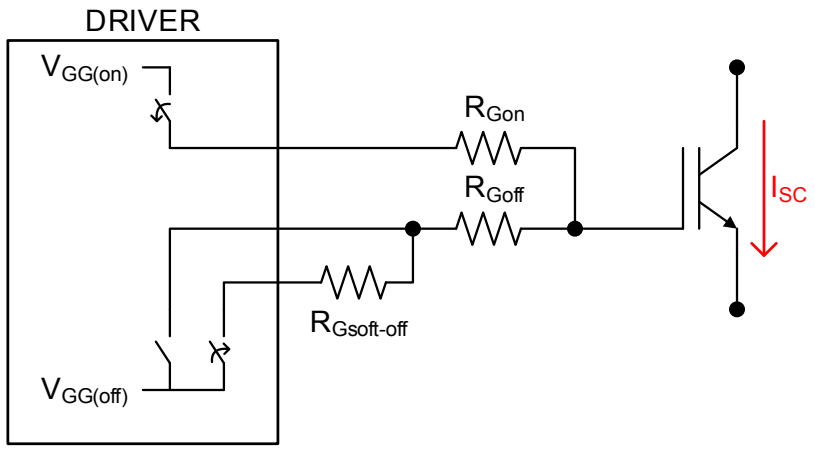
4.2 Internal gate resistor

Many power modules have an internal gate resistance, R_{Gint}, for each switch installed inside the module or, more often, fabricated directly onto the IGBT/MOSFET die. This resistor is added by the manufacturer to stabilize the switching behaviour of the device and cannot be removed or changed. Furthermore, all datasheet values for switching losses, switching speeds, etc. already account for this resistance. Therefore, all "R_G" values give on the datasheet are for external, user-applied gate resistors. The internal gate resistor is only used for calculating peak gate current (3.4) and estimating gate current pulse width (4.3).

4.3 Soft turn-off resistor

Many drivers offer dynamic short-circuit protection (DSCP, V_{CE}-monitoring, DESAT) where the secondary side of the driver can detect a rise in the on-state voltage of a device due to a short circuit and immediately switch off the device. However, turn-off at high current with the "normal" gate resistor can lead to overvoltage across the device. Therefore, many DSCP circuits incorporate an additional soft turn-off resistor that is put in series with the normal R_{Goff} in the event of a DESAT event (Figure 10). This increased turn-off resistance is intended to slow the turn-off of the device, thereby reducing the rate of change of current and hence the induced overvoltage.

Figure 10: Soft turn-off resistor during DESAT event

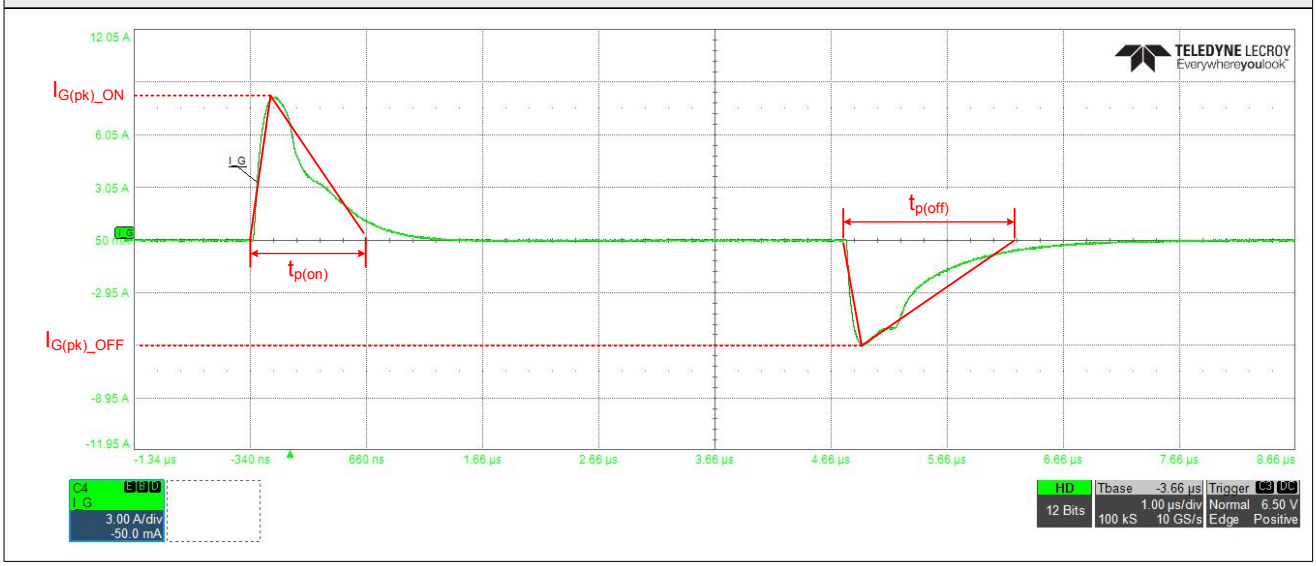


A typical starting value for $R_{Gsoft-off}$ is 10 times R_{Goff}. However, the proper value has to be very carefully evaluated in the system in accordance with the individual application parameters. The setup is a balance between staying within the maximum permitted short circuit time of the device (t_{psc}) while also not exceeding the voltage limit (V_{CES} or V_{DSS}).

4.4 Power dissipation

A high peak gate current (3.4) passes through the gate resistor during each switching transition at a frequency typically in the kHz range. This results in a large amount of power dissipated in a small (typically surface mounted PCB) resistor. Figure 11 illustrates the shape of the current at the gate, with positive pulses flowing through the turn-on resistor and negative pulses flowing through the turn-off resistor.

Figure 11: Gate current waveform



If the shape of the current pulses is assumed triangular, the RMS value and hence, the average power dissipation in either the turn-on or the turn-off resistor can be calculated:

$$P_{R\_G\_avg} = \left(I_{G(pk)} \cdot \sqrt{\frac{t_p \cdot f_{sw}}{3}}\right)^2 \cdot R_G \qquad (4)$$

Where:

$I_{G(pk)}$: Either turn-on or turn-off peak current
f_{sw}: Switching frequency in Hz
R_G: Either turn-on or turn-off gate resistor
t_p: Either turn-on or turn-off current base width (as defined in Figure 11), which can be estimated as:

$$t_p \approx \frac{2 \cdot Q_g}{I_{G(pk)}} \qquad (4b)$$

As the peak currents can be quite high, it is also critical to consider the peak power dissipated in each resistor:

$$P_{R\_G\_pk} = I_{G(pk)}^{\ 2} \cdot R_G \qquad (5)$$

Resistors manufacturers should provide a graph of repetitive pulse load capability (in W) versus pulse duration (in s).

4.5 Resistor type

The high power dissipated in the gate resistors requires consideration of the resistor's power rating, particularly for modern surface mount types. Furthermore, the relatively low resistance values, high operating temperature, and high pulse current capability are generally found in metal film resistors, and in particular, the cylindrical Metal Electrode Leadless Face (MELF) type.

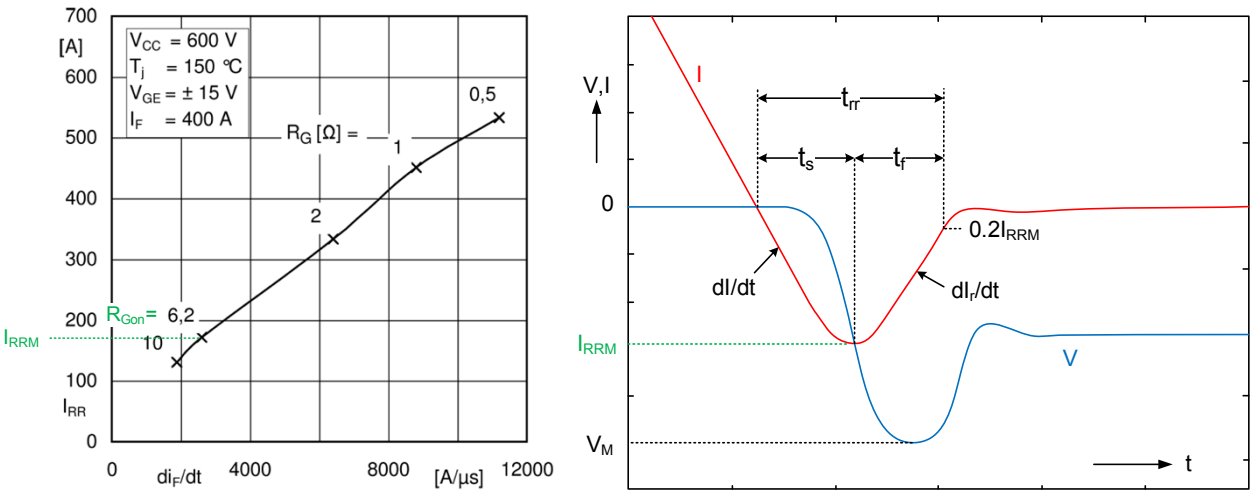
Lastly, the high power requirements, coupled with the fact that failure (opening) of a gate resistor could cause the IGBT or MOSFET to remain on, means that most high power converter designs utilize multiple resistors in parallel to achieve the effective R_{Gon} or R_{Goff} value. In this way the heat can be spread across a PCB and the failure of a single gate resistor does not necessarily mean control of the converter is immediately lost.

4.6 Switching behaviour of the free-wheeling diode

The switching behaviour of the free-wheeling diode is also affected by the gate resistor and limits the minimum value of the gate resistance. This means that the turn-on switching speed of the IGBT can be only increased up to a level compatible with the reverse recovery behaviour of the free-wheeling diode being used. Figure 12 depicts the typical dependency of the free-wheeling diode reverse recovery current IRRM on

di_F/dt, determined by the control of the given gate resistor R_{Gon} of the IGBT. The reverse recovery current increases with the commutation speed, di_F/dt. An increase in I_{RRM} will also cause higher turn-off power dissipation in the free-wheeling diode. Using a turn-on resistor above the minimum recommended value (4.1) will reduce such behaviour.

Figure 12: Diode peak reverse recovery current vs. di/dt and R_{Gon} (L) and soft recovery (R) (SKM400GB12E4)

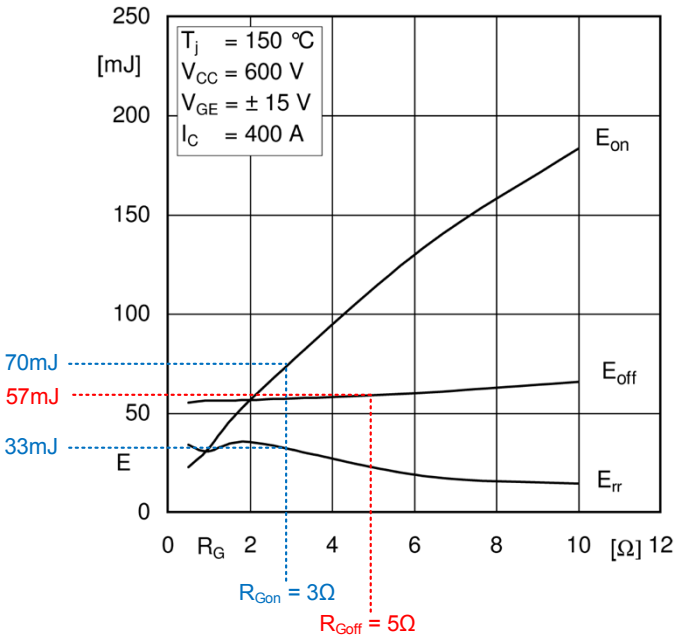


4.7 Influence on switching losses

While it is generally safe to assume that higher gate resistor values lead to slower switching speeds and higher switching losses, the actual effect of gate resistance on switching loss is defined more clearly using a graph on the device datasheet (Figure 13). The slope and shape of these curves can vary dramatically between device generations.

The example figure also illustrates the consideration for differing turn-on and turn-off resistor values. The turn-on resistor (R_{Gon}) determines the turn-on energy of the IGBT/MOSFET as well as the turn-off (reverse recovery) energy of the corresponding freewheeling diode. The turn-off resistor (R_{Goff}) determines only the turn-off energy of the IGBT/MOSFET.

Figure 13: Effect of gate resistors on switching energies (SKM400GB12E4)

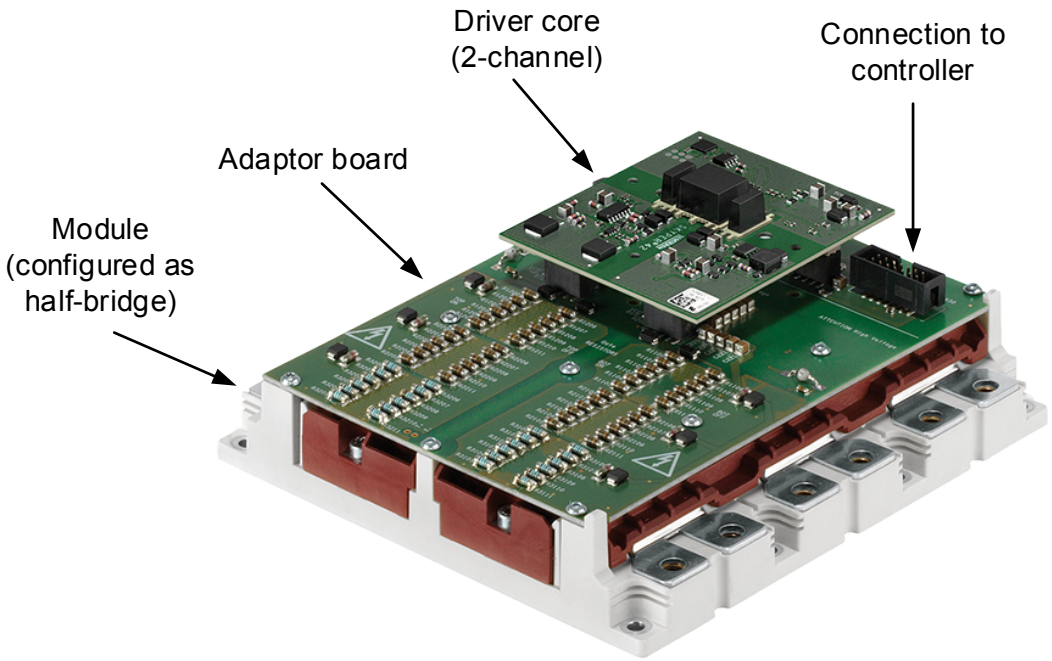


5. Physical Implementation

Equally important to individual component values is the physical layout of the driver. In the case of a driver core, the user is responsible for constructing an adaptor board which contains the application specific components (e.g. gate resistors), configuration components for the driver (e.g. for selecting dead time, DESAT protection levels), and connections to the power module (e.g. solder, spring, plug, wire). This combination of driver core plus adaptor board(s) then becomes the "gate driver" circuit. An example is given in Figure 14 where a SKiM93 module is being driven by a SKYPER 42 driver core. A "Board 93 GB SKYPER 42 R" is used for the adaptor board and provides connections to the driver, turn-on and turn off gate resistors, and a connector for connection to the PWM controller. In this case, the board also serves to parallel each set of three IGBTs in the module, allowing a "6-pack" (three individual half-bridges) to operate as a "2-pack" (single large half-bridge).

In certain instances (smaller power applications), the controller may be integrated into the same circuit board as the driver, however, physical separation of some sort must be still maintained, at least for the sake of voltage isolation.

Figure 14: Example of SKiM93 module with SKYPER 42 driver core and adaptor board

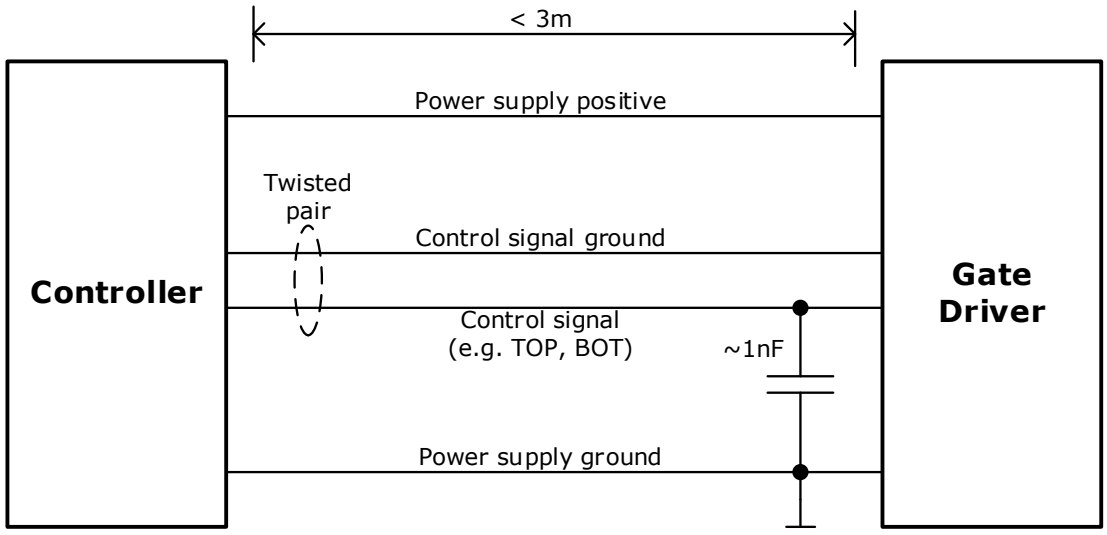


5.1 Connections between controller and driver

Control signals for the gate driver cannot be compromised by interference. Electrical interference can come from a number of sources such as high di/dt and dv/dt due to IGBT/MOSFET switching. The primary goal is then to minimize coupling between the control signals and these noise sources. A few design tips for gate driver / controller connection are given below:

- Traces on the printed circuit board should be kept as short as possible. Loops (large areas between a signal and its return) should be avoided.
- Cables from the controller should not exceed three meters. Twisted pair cable should be used.
- Control signals should not be grouped with control power supply lines. Signal grounds and power supply grounds should be separate. Both grounds should be tied at a single point to avoid ground loops.
- Signal cables should be placed as far away as possible from power terminals, power cables, ground cables, DC-link capacitors and all other noise sources.
- Control signal cable should not run parallel to power cable. The minimum distance between control signal cable and power cable should be 30cm and the cables should only cross perpendicularly.
- It is recommended that all cables be kept close to ground (e.g. heat sink or similar).
- In noise intensive applications, it is recommended that shielded cables or fibre optic interfaces be used to improve noise immunity.
- Use a low value capacitor (1nF) between signal and power supply ground of the gate driver for differential mode noise suppression. With current limited line drives, this capacitor can cause a small delay of a few ns.
- The use of an open-collector driver from the controller for the gate signals is not recommended.

Figure 15: Connections between controller and gate driver



5.2 Connections between driver and module

The gate driver must be located very close to the module to minimize stray inductance. An advantageous solution, even for high-power modules, is to mount the gate driver onto the IGBT module directly. Where this is not possible, at least the components shown in Figure 16 should be mounted at the module (e.g. on a small auxiliary circuit board) with cabling run up to the driver board. A few design tips on gate driver/IGBT connection for systems where wire connections are used are given in the following sections.

5.2.1 Lead dress

- The connections between gate driver and module must be kept as short as possible. Gate and emitter wiring should be twisted pair.
- Gate wiring for top and bottom IGBTs or other phases must not be bundled together.
- The V_{CE}-monitoring (DESAT protection) wiring must not be bundled together with the gate and emitter wiring.
- Voltage is induced across L_E (Figure 16) due to the high di/dt of the load current. If the ground (emitter connection) of the driver circuit is connected to this power terminal (instead of the auxiliary emitter), the voltage across L_E decreases the gate turn-on voltage. In addition, voltage is added to the gate turn-off voltage to slow down turn-on/turn-off. Use auxiliary emitter contacts to minimize the negative feedback effect on gate-emitter voltage.
- The total stray inductance in the gate-emitter circuit (combination of LG values in Figure 16) forms an LC circuit with the gate input capacitance C_{ies}. The resonation of this LC circuit could cause voltage peaks exceeding the rating of the device. In order to damp these oscillations, it is suggested that the gate resistor be no smaller than:

$$R_{G(min)} \geq 2 \cdot \sqrt{\frac{L_{G\_total}}{C_{ies}}} \qquad (6)$$

  A high gate inductance can also inadvertently accelerate switching speed which may cause a device to operate outside its safe operating area (i.e. collector-emitter overvoltage).

5.2.2 Component location

- Place the gate resistances for turn-on and turn-off close together.
- If external boost capacitors are used, the capacitors must be placed as close to the gate driver as possible in order to minimize parasitic inductance.

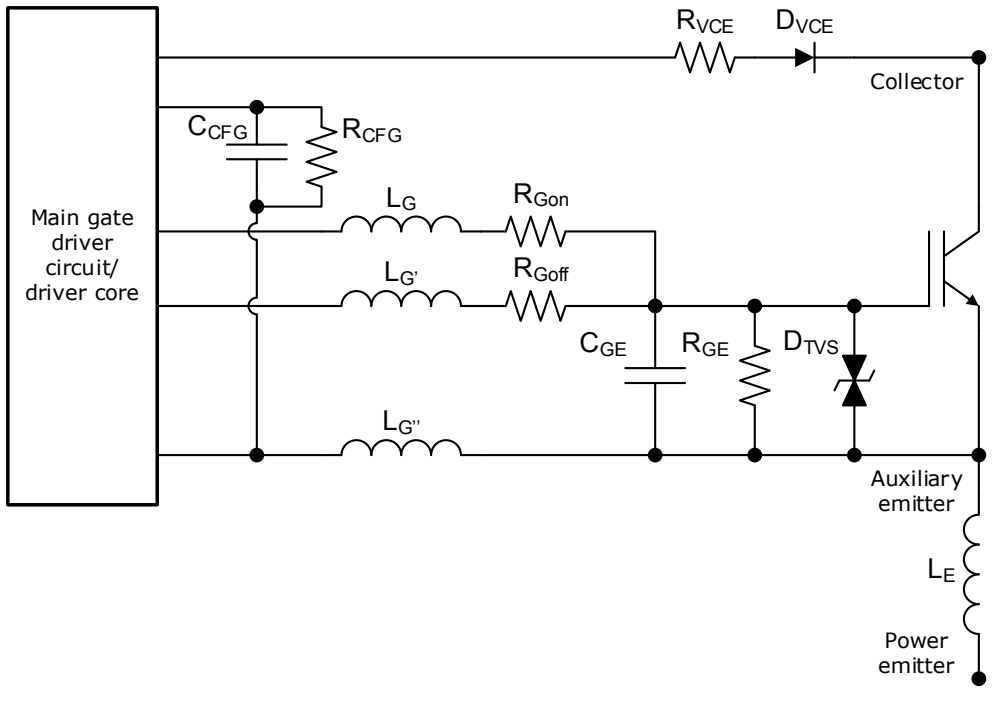
5.2.3 Additional components

- In order to ensure an IGBT remains off when the driver supply voltage is removed and voltage is applied to the power circuit it is recommended that a 10kΩ resistor (R_{GE}) be placed between the gate and emitter. If a wire connection is used, do not place R_{GE} between printed circuit board and IGBT module. R_{GE} has to be placed very close to the module.
- Use a transient voltage suppressor (D_{TVS}) between gate and emitter. The suppressor diode must be placed very close to the IGBT module and can protect the IGBT gate in overvoltage conditions as well as limit the short circuit current should a short circuit occur. During short circuit, the gate emitter voltage may increase due to the Miller capacitance between collector and gate. High dv/dt during short circuit causes a current to flow through the Miller capacitor, in doing so increasing the gate emitter voltage. The suppressor diode will clamp this voltage. Furthermore, the suppressor diode can protect the gate driver from consequential damage should the IGBT module malfunction.
- The use of a capacitor (C_{GE}) between gate and emitter can be advantageous, even for high-power IGBT modules and parallel operation (see [5]). The gate emitter capacitor C_{GE} is used as a smoothing capacitor, especially in the event of a short circuit, in order to reduce oscillation at the IGBT gate. C_{GE} should be approximately 10…50% of the intrinsic C_{GE} of the IGBT. The C_{GE} has to be placed very close to the IGBT module.
- Driver circuits (such as the SKYPER series) that incorporate V_{CE}-monitoring (DESAT protection) monitor the collector-emitter voltage when the device is in an on state. When the device is off, a diode (D_{VCE}) is necessary to block high voltage from damaging the driver. This diode must be capable of blocking at least the same voltage as that of the main device. Additionally, the diode must have a reverse recovery time faster than the V_{CE} rise time of the main device. These requirements, coupled with the necessary voltage spacing, limit the selection to specialized diodes such as the BY203 series. For higher voltage operation (e.g. with 1700V devices), an additional resistor (R_{VCE}) is used to further reduce the voltage. The voltage drops of these additional components need to be considered when selecting the trip point for the V_{CE}-monitoring circuit.

  The trip point (V_{CEStat}) for the V_{CE}-monitoring is typically set through a resistor (R_{CFG}) that forms the lower half of a voltage divider. A capacitor (C_{CFG}) in parallel determines the blanking time (t_{bl}) for the detection circuit.

  Further details for selecting component values are given in the respective Technical Explanations document for the driver core.

Figure 16: Connections between gate driver and module (one channel shown)

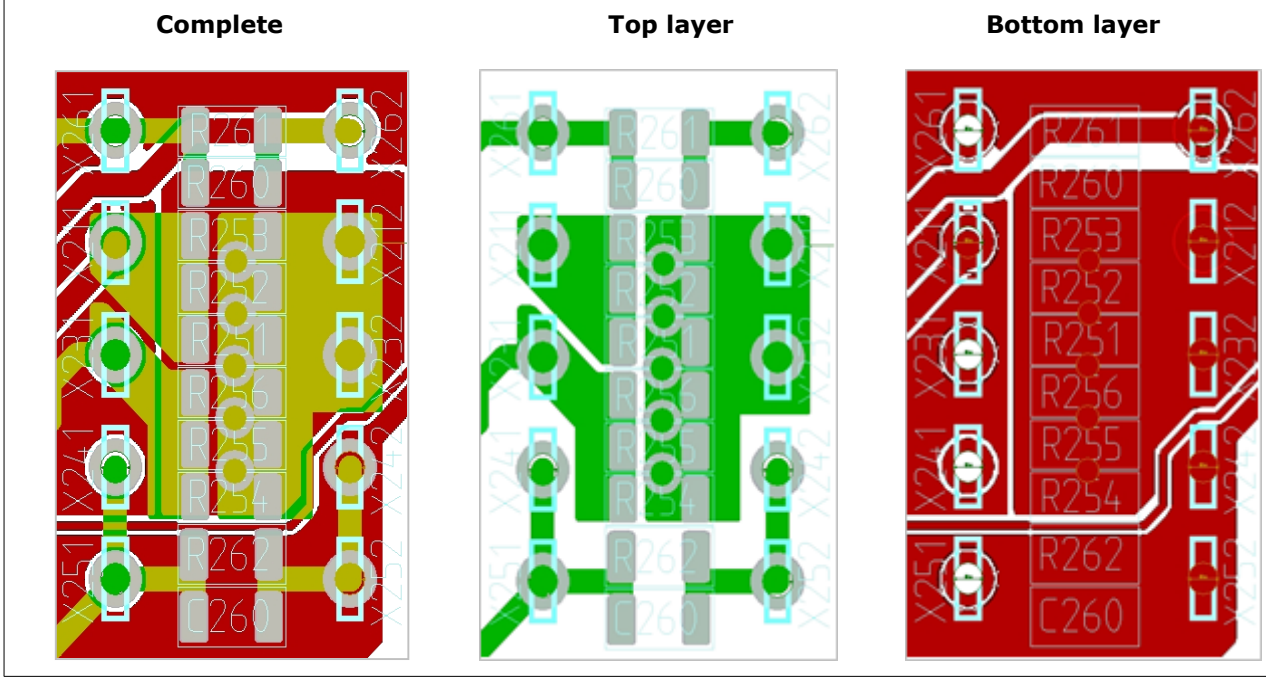


5.3 PCB layout

The thermal requirements for the gate resistors described in 4.3 and 4.5, coupled with the bullet points in 5.2, dictate the layout of the PCB. The primary guiding point is the use of a large emitter plane at least beneath the gate resistors. This technique reduces stray inductance and provides some heatsinking.

Figure 17 shows a layout for turn-on and turn-off resistors with an emitter plane. The left side of the figure shows the complete layout with R_{Gon} (R251//R252//R253) and R_{Goff} (R254//R255//R256) in the centre. The centre of Figure 17 shows the topside connection for the resistors with large areas of copper providing heatsinking (note that the pads extend beneath the resistors). The right of Figure 17 shows the large emitter plane on the copper layer below the topside layer, extending below the resistors and reducing any loop area that would cause parasitic inductance in the gate-emitter circuit.

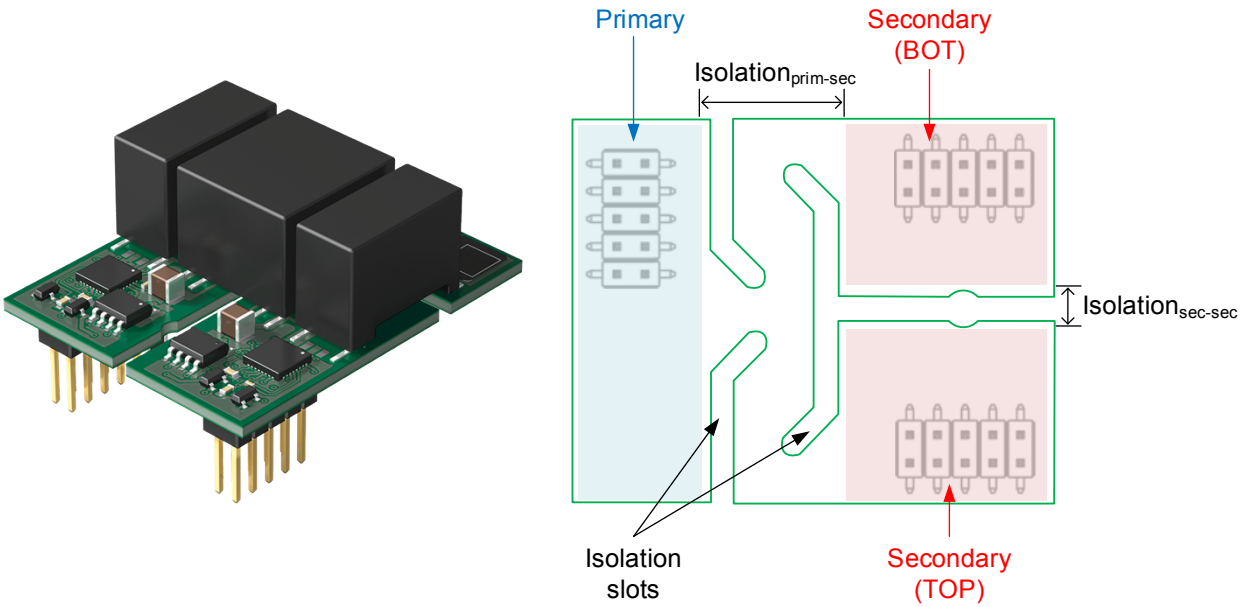
Figure 17: Example PCB layout for gate resistors



5.3.1 Insulation coordination

When designing a PCB for a driver core, it is important not to compromise the isolation voltage rating of the system by reducing creepage and clearance distances below those defined by the driver core itself. For example, most two-channel SKYPER driver cores are divided into "islands" of isolated circuits, each with their own connectors down to the main PCB (Figure 18). These driver cores may also include slots to increase creepage distance; these notches do not necessarily need to be duplicated on the PCB if care is taken to separate circuits.

Figure 18: Isolation concept on SKYPER 12 PV driver core



Further information regarding standards and methods for determining insulation coordination can be found in [8].

6. Conclusion

Gate driver design is a complex topic but driver products are commercially available that allow a user to focus on tuning the operation of the power module. Initial sizing of such a driver can be quickly performed as shown here but no closed-form formulae can give the perfect component values for a particular application. Thorough lab testing (e.g. double-pulse testing, [4]) is required to arrive at final gate resistor values.

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